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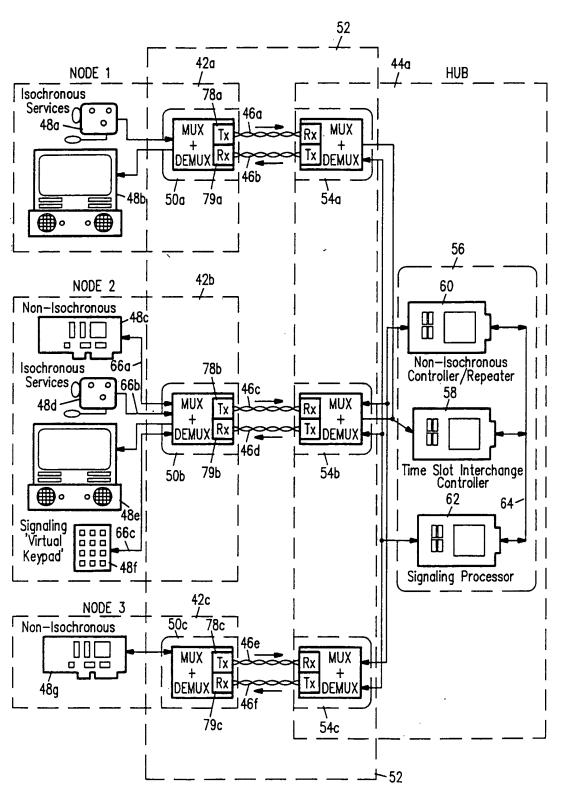


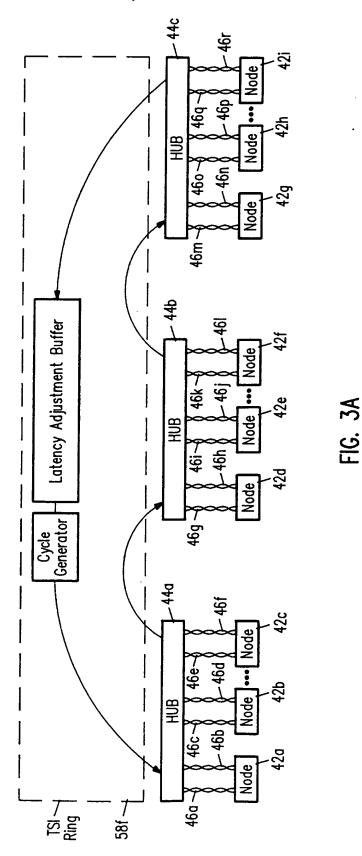
FIG. 2

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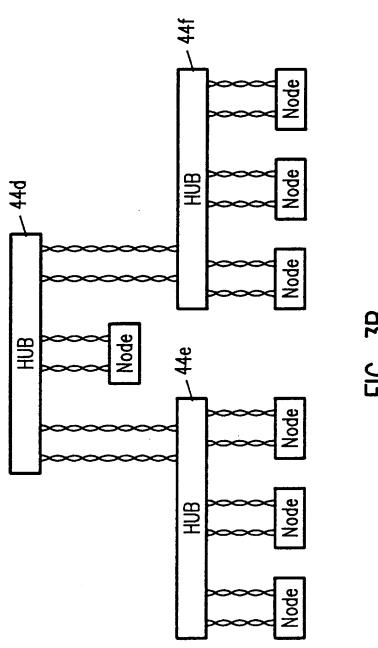
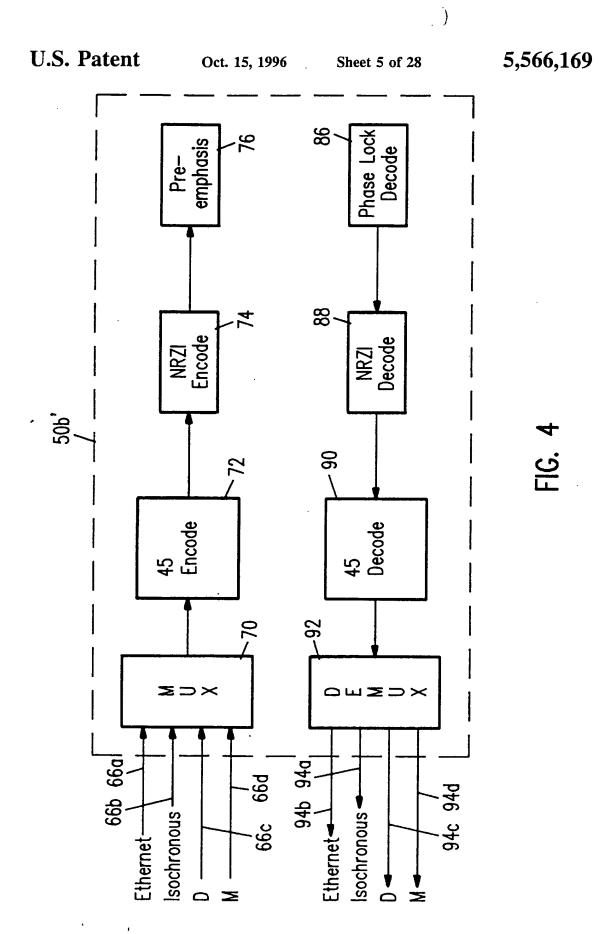
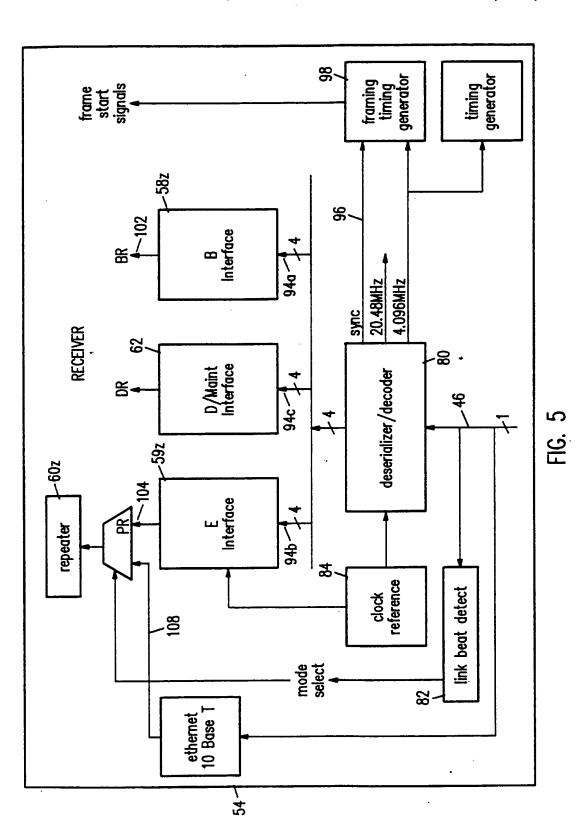


FIG. 38





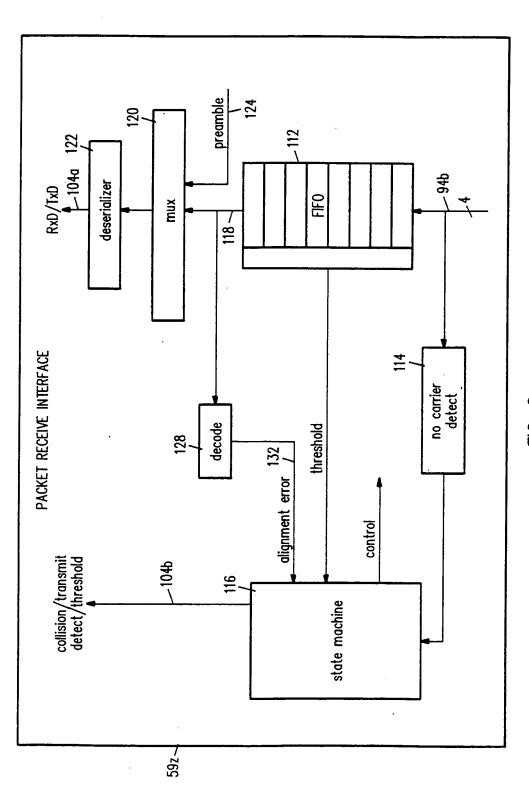


FIG. 6

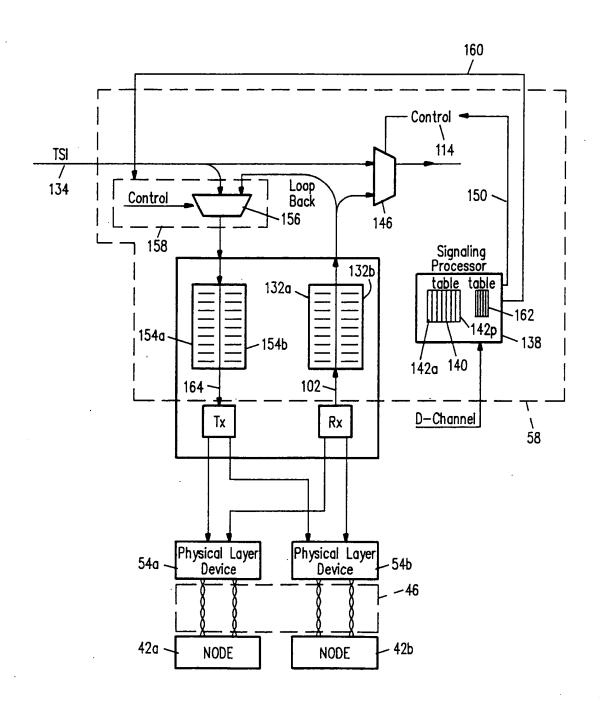


FIG. 7

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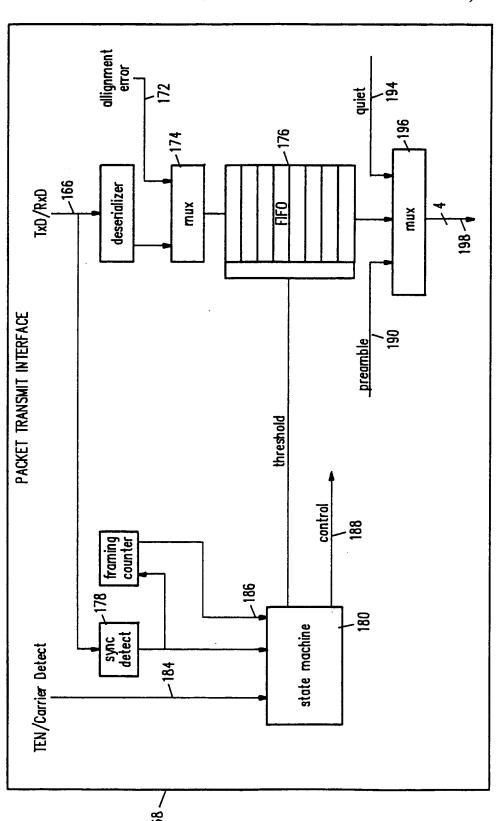


FIG. 8

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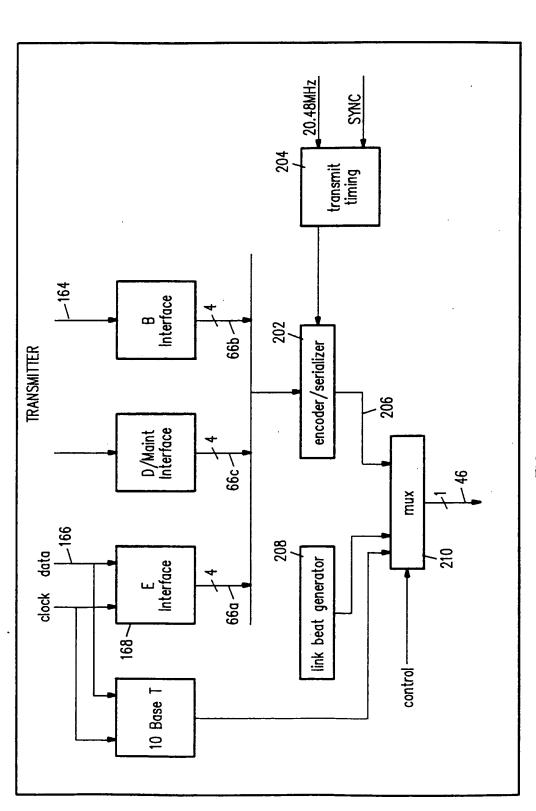
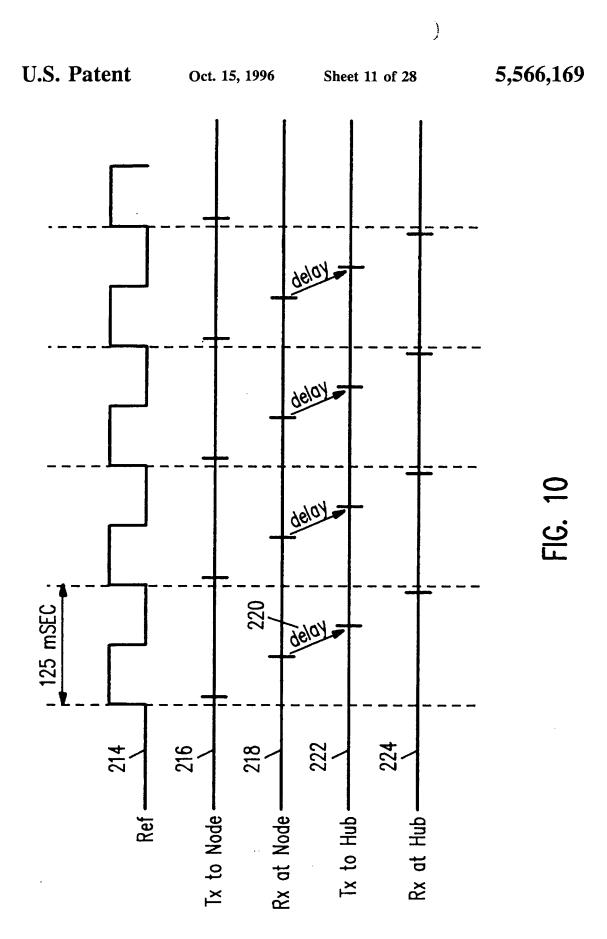


FIG. 9

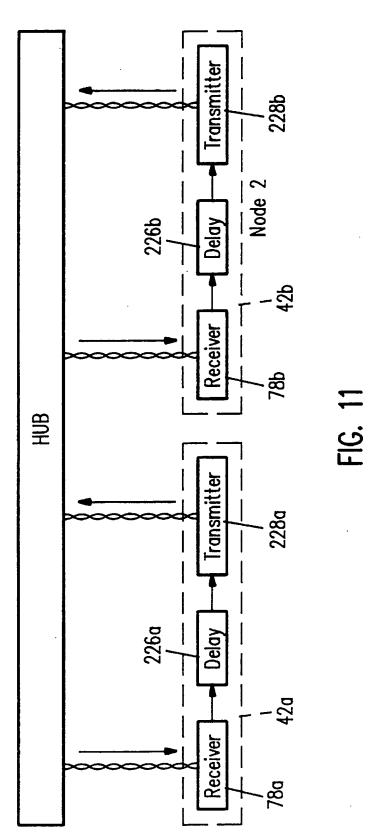




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U.S. Patent 5,566,169 Oct. 15, 1996 **Sheet 13 of 28** - 54p' **Diagnostics** Diagnostic Control Register Processor Interface Physical Layer Device 15 51210 ⊼ Buffer TX Datapath • 1224 1226 Cascade Control OCR Reg Port Reg RX Shift Control 1218 1219 RX Datapath 54b RX Buffer Physical Layer Device FRAME Diff Physical Layer Device IFR GEN 1214

1204 TSI Delm

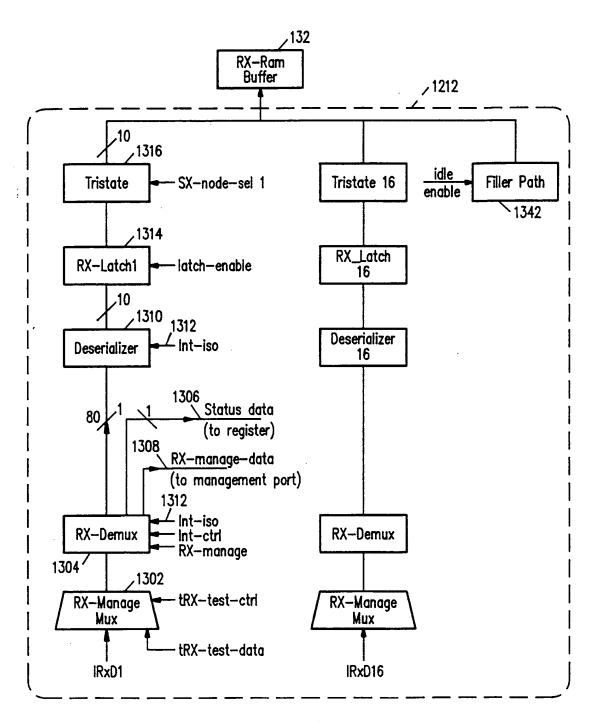


FIG. 13

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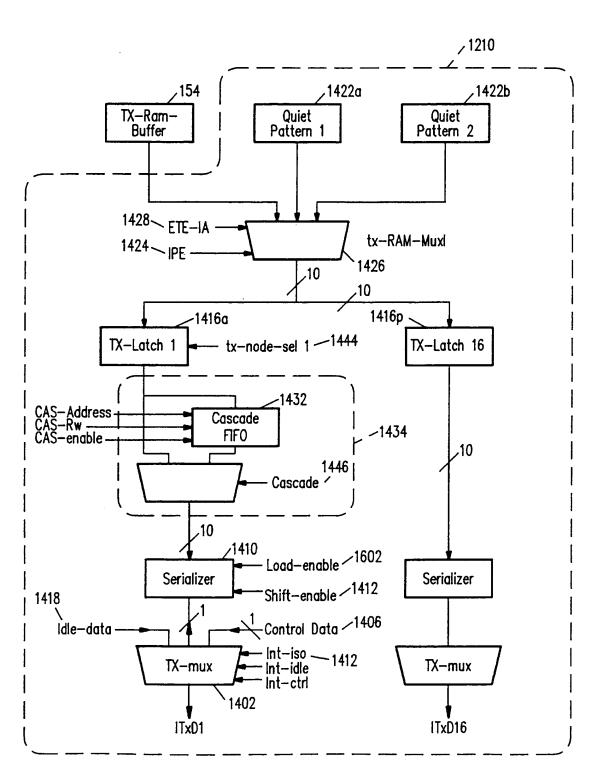


FIG. 14

5,566,169 U.S. Patent Oct. 15, 1996 Sheet 16 of 28 1215 IFR 8 6 10 10 **RXD** B96 | IDLE | IDLE | STAT | STAT | B1 | IDLE | B2 | IDLE | B3 | 2560 Clock Cycles -125 us TXD: Data sent from Isochronous Data Exchanger to Physical Layer Portion. Data Received by Isochronous Data Exchanger from RXD: Physical Layer Portion. Isochronous Frame Sync signal sent from Isochronous IFR: Data Exchanger to Physical Layer Portion. CTRL: Control data sent from Isochronous Data Exchanger to Physical Layer Portion. Status data sent from Physical Layer Portion to STAT: Isochronous Data Exchanger. B(1:96): B channel data (96 bytes of Bchannel data per us cycle). Filler data. IDLE: FIG. 15A Ring Frame: 12.5 MHz Preamble 2/3 1548 1 12 1 C-H Phy Frame: 20.48 MHz FIG. 15B

C-H

15

20 25

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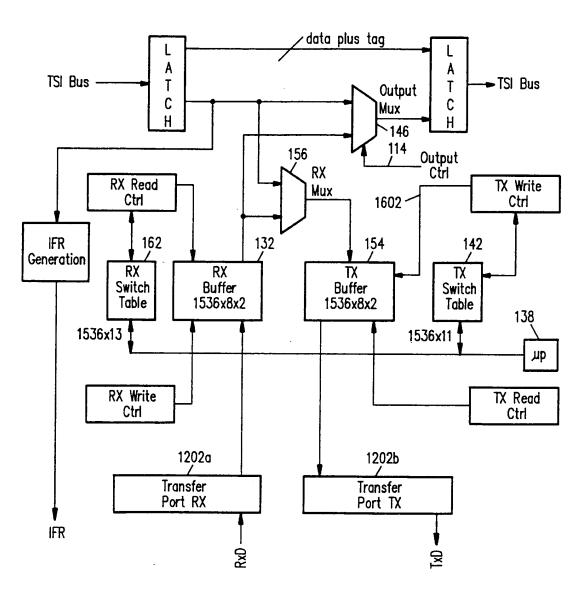
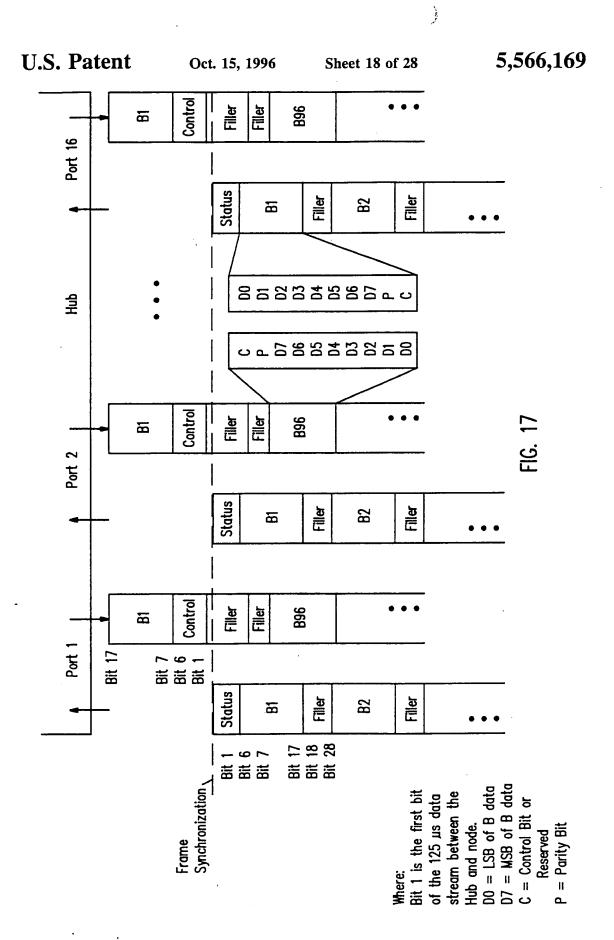


FIG. 16



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KE2 Control Data Transmitted **KE2 BE2 KE2 KE2**

CY2 Status Data Received Mdl CVb DINT

器 5

Control Bits

Reserved bit. RES:

Status Bits

Cascade bit: Used to activate the port 1 cascade logic. CAS:

Link Active: Indicates that the link is isochoronous active when set.

Low Power Mode: Indicates that the isophy is in low power mode when set.

CAPacity. Indicates the type of Isochronous capacity. "1" 15.872 Mbps Isochronous bandwidth "0" 6.144 Mbps Isochronous bandwidth

CAP:

PM

₹

D INTerrupt: Indicates that the isophy has received a start of D channel packet when set. OIN T

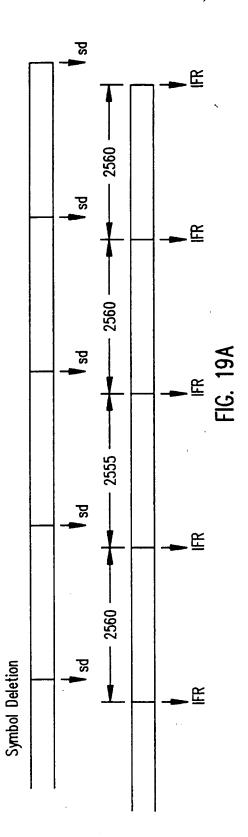
M INTerrupt: Indicates that the isophy's maintenance has changed when set. PIN T

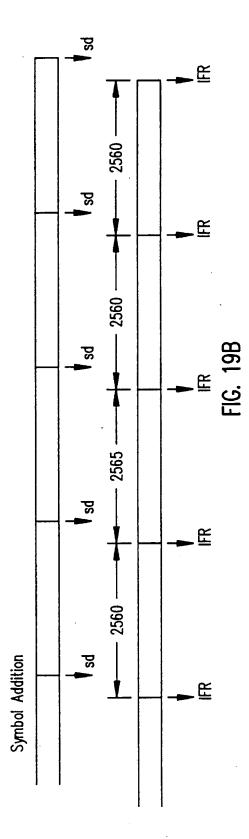
U.S. Patent

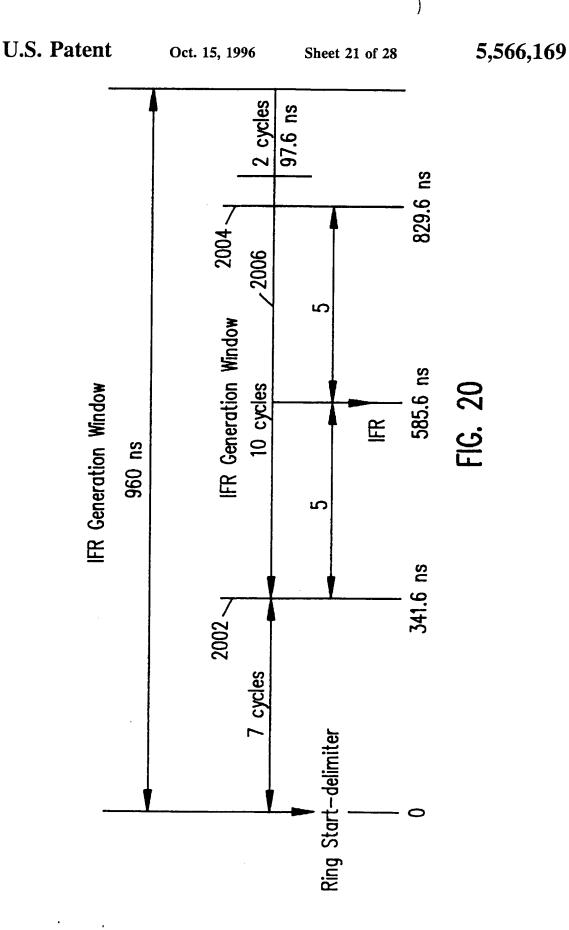
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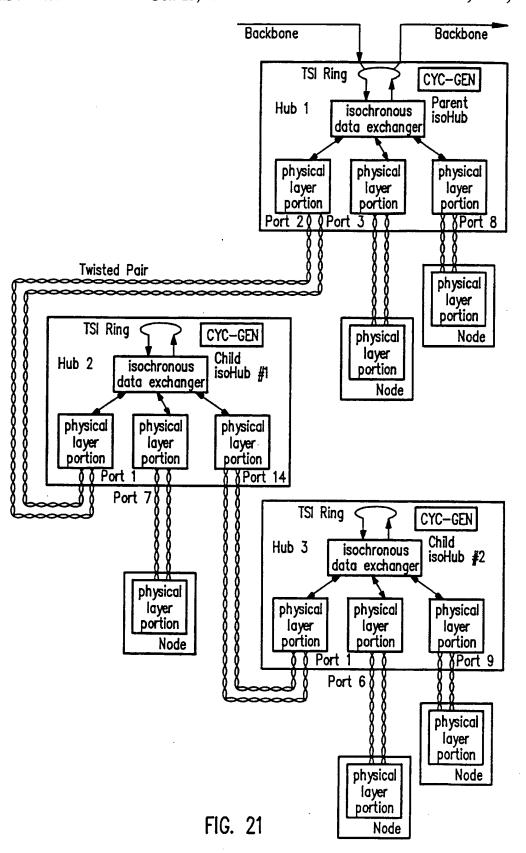


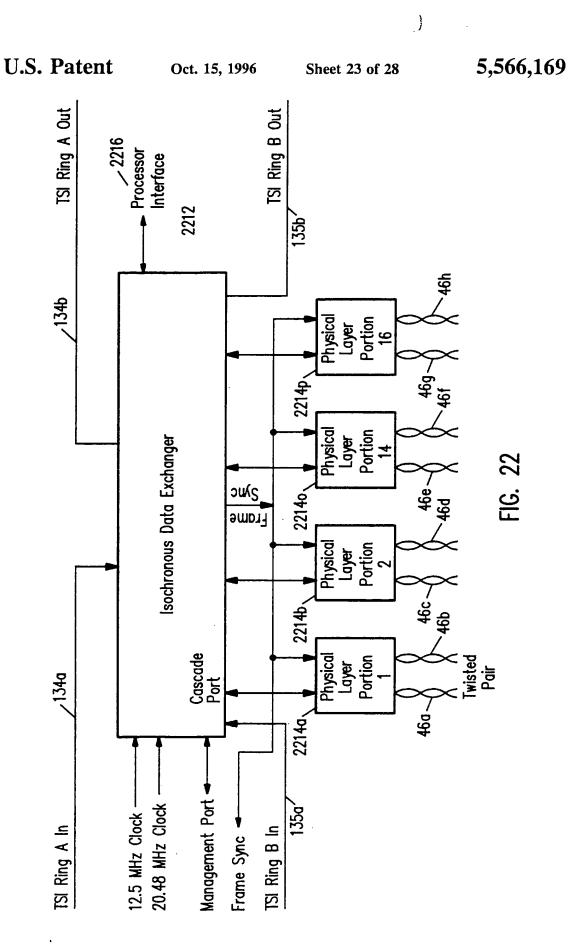
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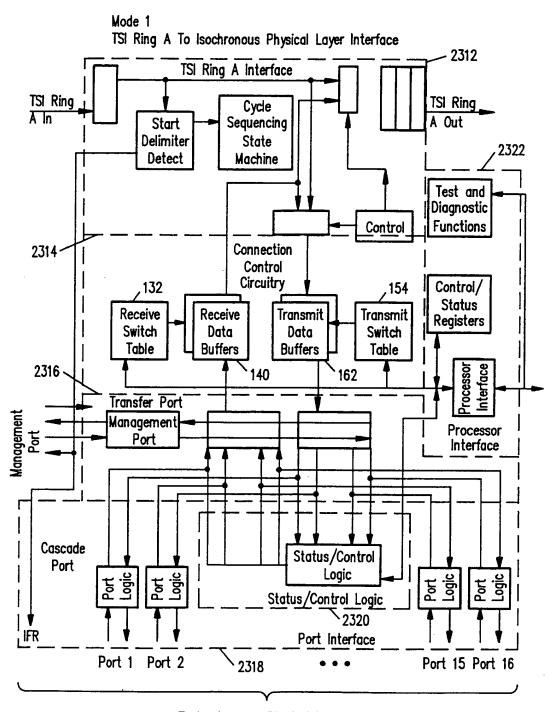
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To Isochronous Physical Layer

FIG. 23A

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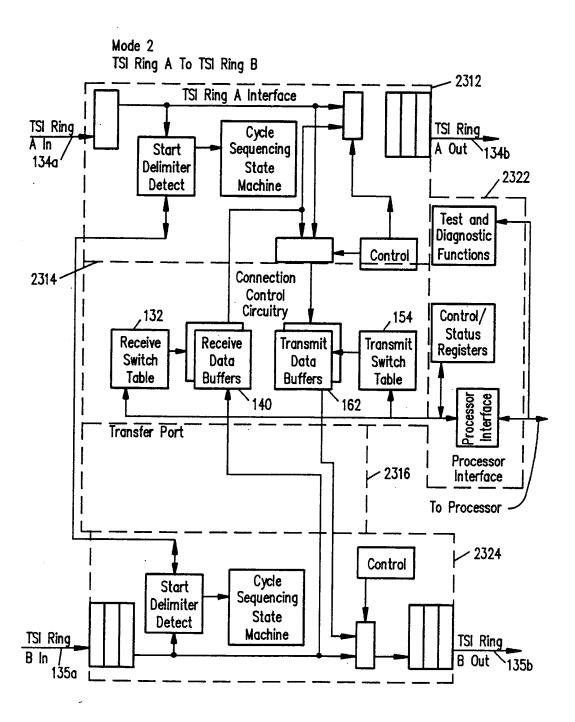


FIG. 23B

, i accit	Oct. 15, 1996		S	heet 2	5,566	
Switch Table Address		Receive	e Switch	n Table		
Isochronous Maintenance Channel (IMC)	e 0	Parity	TSE	ITE	ЕТЕ	Data Buffer Address
TSI Ring A Slot 1	1					
TSI Ring A Slot 2	2					
•	•				,	•
TSI Ring A Slot 1535	1535					
TSI Ring A Slot 1536	1536					,
		MSB 1 Bit	1 Bit FIG.	1 Bit 24A	1 Bit	LSB —— 11 Bits ——
Switch Table Address		Transm				
			iit Swit	ch labi	е	-
Not Used	0	Parity	Not Used	ch labl	e IA	Data Buffer Address
	0		Not	r	1	Data Buffer Address
Not Used Port 1, B channel 1 Port 2, B channel 1	-		Not	r	1	Data Buffer Address
Port 1, B channel 1	1		Not	r	1	Data Buffer Address
Port 1, B channel 1 Port 2, B channel 1	1		Not	r	1	Data Buffer Address • • •
Port 1, B channel 1 Port 2, B channel 1 Port 14, B channel 96	1 2		Not	r	1	Data Buffer Address • • •
Port 1, B channel 1	1 2 • • •		Not	r	1	Data Buffer Address LSB

ITE:Internal Transmit Enable:

IA: Idle Address:

Indicates the idle pattern to be sent.

IPE:Idle Pattern Enable:

Indicates on Internal loopback of the slot when set. Indicates the use of a quiet pattern when set.

U.S. Patent 5,566,169 Oct. 15, 1996 **Sheet 27 of 28** Switch Table Address Receive Switch Table Isochronous Maintenance Parity 0 Channel (IMC) TSE ITE ETE Data Buffer Address TSI Ring A Slot 1 . 1 TSI Ring A Slot 2 2 TSI Ring A Slot 1535 1535 1536 TSI Ring A Slot 1536 **MSB** LSB 1 Bit 1 Bit 1 Bit 1 Bit -– 11 Bits — 🖚 FIG. 25A Switch Table Address Transmit Switch Table

Switch lable Address	Iransmit Switch Table						
Isochronous Maintenance Channel (IMC)	0	Parity	TSE	Not Used	ETE	Data Buffer Address	
TSI Ring B Slot 1	1						
TSI Ring B Slot 2	2						
•	•					•	
TSI Ring B Slot 1535	1535						
TSI Ring B Slot 1536	1536						
		MSB 1 Bit	1 Bit	1 Bit	1 Bit	LSB LSB	
Bit Definitions		į	FIG.	25B			

Bit Definitions

ETE: External Transmit Enable:

In Mode 2, indicates an External switching of

slot when set.

TSE: Tri-State Enable:

The isoTSX drives the TSI ring output drivers

when set.



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